Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Flip-chip BGA package assembly transfer from SCC to JSCC for STIH310 products.
PCN Reference : MDG/17/10000

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STIH410-EJB	STIH301-SNB	STIH310-PJB
STIH310-YJB	STIH305-YJC	STIH310CYJB
STIH312-DJB	STIH312-SJB	STIH412-DJB
STIH301CRNB	STIH407-BJC	STIH305-BJC
STIH310-DJB	STIH412-BJB	STIH310CKJB
STIH410-DJB	STIH412DHJB	STIH301CVNB
STIH410-LJB	STIH301CYNB	STIH410-BJB
STIH301-BNB	STIH310CBJB	STIH412-HJB
STIH412-SJB	STIH312-YJB	STIH412-EJB
STIH310-EJB	STIH310CSJB	STIH310-IJB
STIH310CTJB	STIH301CPNB	STIH310-NJB
STIH301-DNB	STIH310-SJB	STIH312-LJB
STIH410-VJB	STIH310-BJB	STIH301CMNB

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Reliability Qualification Plan

MDG Back-end qualification DPG0116-QP
JSCC assembly plant
Unmolded FCBGA from 16^2 to 25^2 with Cu pillar
on 28nm LP & FDSOI from SEC

General Information	
Package	*FCBGA 16^2 to 25^2*
Silicon process technology	*28nm LP* *28nm FDSOI*
Bumping	*Copper pillar*
Product division	*ADL*
Affected products	*Cannes 2, Liege2, L2A*

Locations	
Assembly plant location	*Stats-ChipPAC China-JCET plant*
Wafer fab location	*SEC (Samsung)*
Bumping site	*Winstek (former SCT)*
Reliability test location	*ST Grenoble*
Reference number	*DPG0116-QP*

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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS....3
2 GLOSSARY....3
3 RELIABILITY EVALUATION OVERVIEW....3
3.1 OBJECTIVES....3
3.2 DESCRIPTION OF THE CHANGE....4
3.3 STRATEGY FOR THE QUALIFICATION....5
4 PACKAGE CHARACTERISTICS....5
4.1 PACKAGE CONSTRUCTION NOTE....5
4.2 TEST VEHICLES DEFINITION....6
4.3 PACKAGE BALL OUT....6
5 RELIABILITY TEST PLAN....8
5.1 SAMPLE SIZE REQUIRED....8
5.2 LOT DEFINITION....8
5.3 TEST PLAN SUMMARY....8
6 PACKAGE ORIENTED TESTS DESCRIPTION....9

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
DCG/0001/16 **DMS@ST DM00280255**	Qualification request
DMS@ST 8498310	Assembly Flowchart
DMS@ST 8525350	DCG Back-End Qualification Procedure
DMS@ST 0061692	Reliability tests and criteria for product qualification
DMS@ST 8070682	UPD/Wave GNB Reliability qualification procedure
J-STD-020	Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
JESD22-A101	Steady State Temperature Humidity Bias Life Test
JESD22-A102	Accelerated Moisture Resistance - Unbiased Autoclave
JESD22-A103	High Temperature Storage Life
JESD22-A104	Temperature Cycling
JESD22-A110	Highly-Accelerated Temperature and Humidity Stress Test (HAST)
JESD22-A113	Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
JESD22-A118	Temperature Humidity Storage
SOP 2.6.2	Process qualification and transfer management
SOP 2.6.9	Package and process maturity management in Back End
DMS@ST 8470442	POA FCSBGA25x25 (H310-Cannes2)
DMS@ST 8521146	POA FCSBGA19x19 (H310-Liege2)
DMS@ST DM00187128	POA FCBGA16x16 (H32A-L2A)
DMS@ST 8523158	Flip chip diagram (H310-Cannes2)
DMS@ST 8542814	Flip chip diagram (H310-Liege2)
DMS@ST DM00228897	Flip chip diagram (H32A-L2A)

2 GLOSSARY

FCBGA	Flip Chip Ball Grid Array
AFOP	Au on Finger and OSP (organic coating) on ball Pads
MSL JL3	Moisture/Reflow Sensitivity Level test with JEDEC level 3
TC	Thermal cycling
HTSL	High Temperature Storage Life
THS	Temperature Humidity Storage

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification plan is to define the trials to validate the transfer of copper pillar FCBGA lines from Stats-ChipPAC China (SCC) to Stats-ChipPAC China JCET plant (JSCC).

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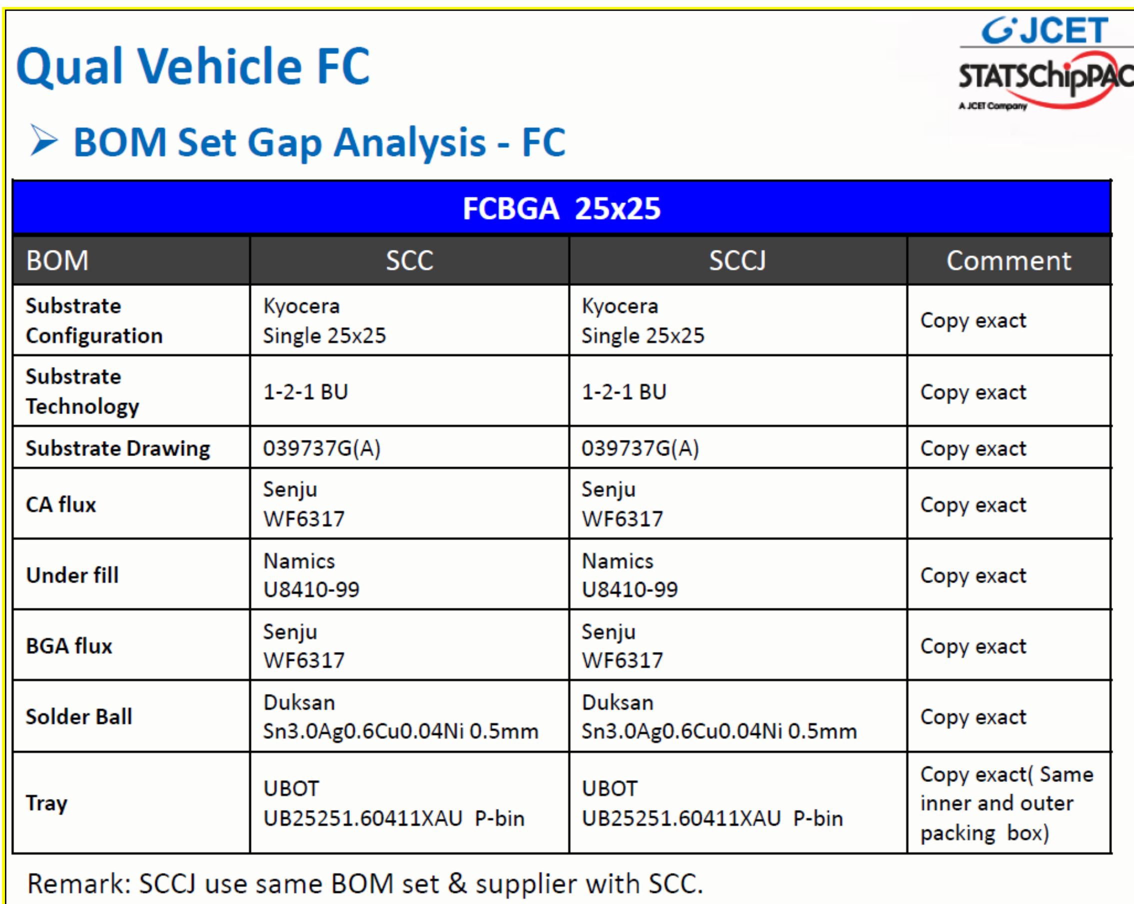
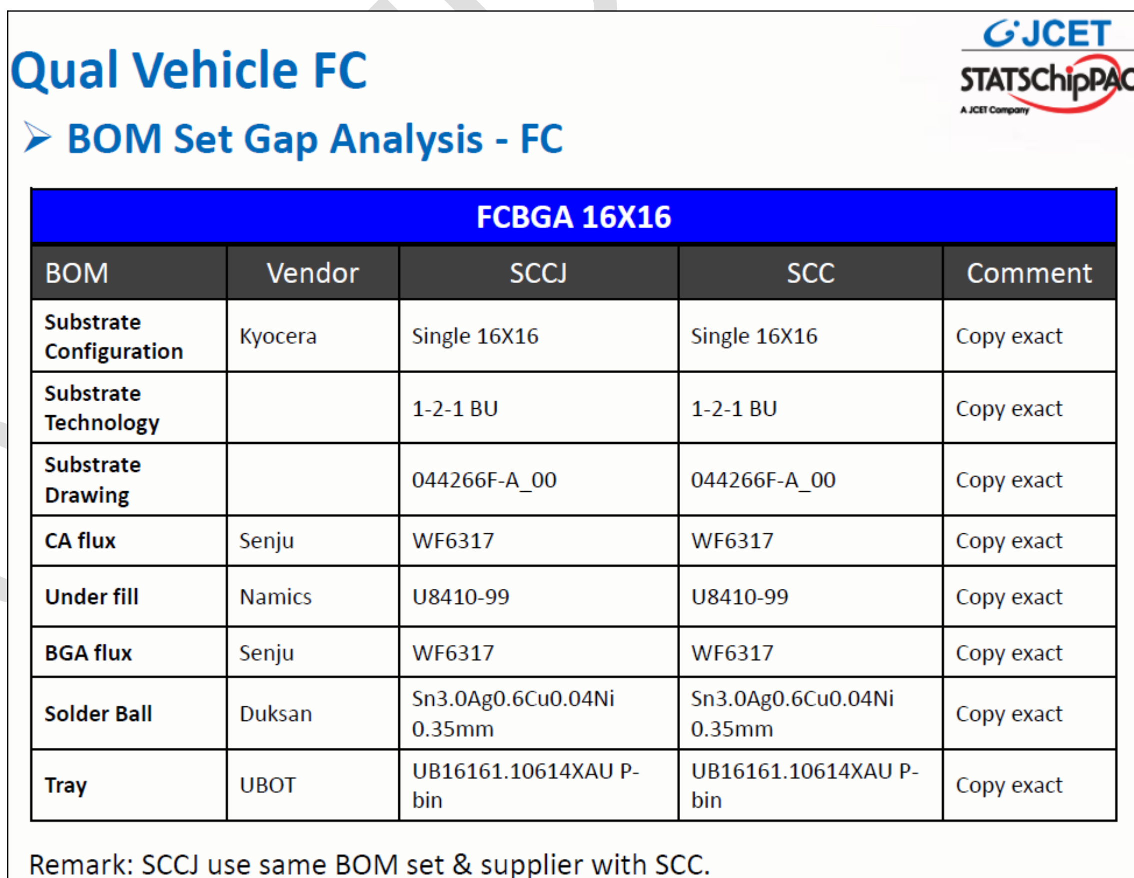
3.2 Description of the change



FCBGA 25x25			
BOM	SCC	SCCJ	Comment
Substrate Configuration	Kyocera Single 25x25	Kyocera Single 25x25	Copy exact
Substrate Technology	1-2-1 BU	1-2-1 BU	Copy exact
Substrate Drawing	039737G(A)	039737G(A)	Copy exact
CA flux	Senju WF6317	Senju WF6317	Copy exact
Under fill	Namics U8410-99	Namics U8410-99	Copy exact
BGA flux	Senju WF6317	Senju WF6317	Copy exact
Solder Ball	Duksan Sn3.0Ag0.6Cu0.04Ni 0.5mm	Duksan Sn3.0Ag0.6Cu0.04Ni 0.5mm	Copy exact
Tray	UBOT UB25251.60411XAU P-bin	UBOT UB25251.60411XAU P-bin	Copy exact(Same inner and outer packing box)

Remark: SCCJ use same BOM set & supplier with SCC.



FCBGA 16X16				
BOM	Vendor	SCCJ	SCC	Comment
Substrate Configuration	Kyocera	Single 16X16	Single 16X16	Copy exact
Substrate Technology		1-2-1 BU	1-2-1 BU	Copy exact
Substrate Drawing		044266F-A_00	044266F-A_00	Copy exact
CA flux	Senju	WF6317	WF6317	Copy exact
Under fill	Namics	U8410-99	U8410-99	Copy exact
BGA flux	Senju	WF6317	WF6317	Copy exact
Solder Ball	Duksan	Sn3.0Ag0.6Cu0.04Ni 0.35mm	Sn3.0Ag0.6Cu0.04Ni 0.35mm	Copy exact
Tray	UBOT	UB16161.10614XAU P-bin	UB16161.10614XAU P-bin	Copy exact

Remark: SCCJ use same BOM set & supplier with SCC.

3.3 Strategy for the qualification

2 Test Vehicles selected:
- Cannes2 / H310 in unmolded FCBGA 25x25 28nm LP SEC
- L2A / H32A in unmolded FCBGA 16x16 28 FDSOI SEC

Cannes2 was previously qualified in SCC and production is running.
Cannes2 being in 2 body sizes 25x25 and 19x19, ST decided to focus on the biggest size 25x25 and to apply a similarity to the smallest 19x19. Indeed there is no difference in baking and humidity trials but the largest body size in TC is generating more stress in 25x25 than in 19x19.

In addition, 2 lots of L2A will be used to complete to cover all packages family.

4 PACKAGE CHARACTERISTICS

4.1 Package construction note

PACKAGE FEATURES			
Macro-package name	FCBGA 25x25	FCBGA 19x19	FCBGA 16x16
Body size (mm²)	25x25	19x19	16x16
Package thickness (mm) (Without solder balls)	0.932		
Pitch (mm)	1.0 (central) & 0.8 (periphery)		0.65
Assembly site	Stats-ChipPAC China JCET		
Substrate finishing	CuOSP		
Substrate layers	1+2+1		
Solder flux for FC attach	Senju WF6317		
Underfill	Namics U8410-99		
Ball attach flux	Senju WF6317		
Solder balls composition	SACN 306		
Solder balls diameter	0.5mm		0.35mm

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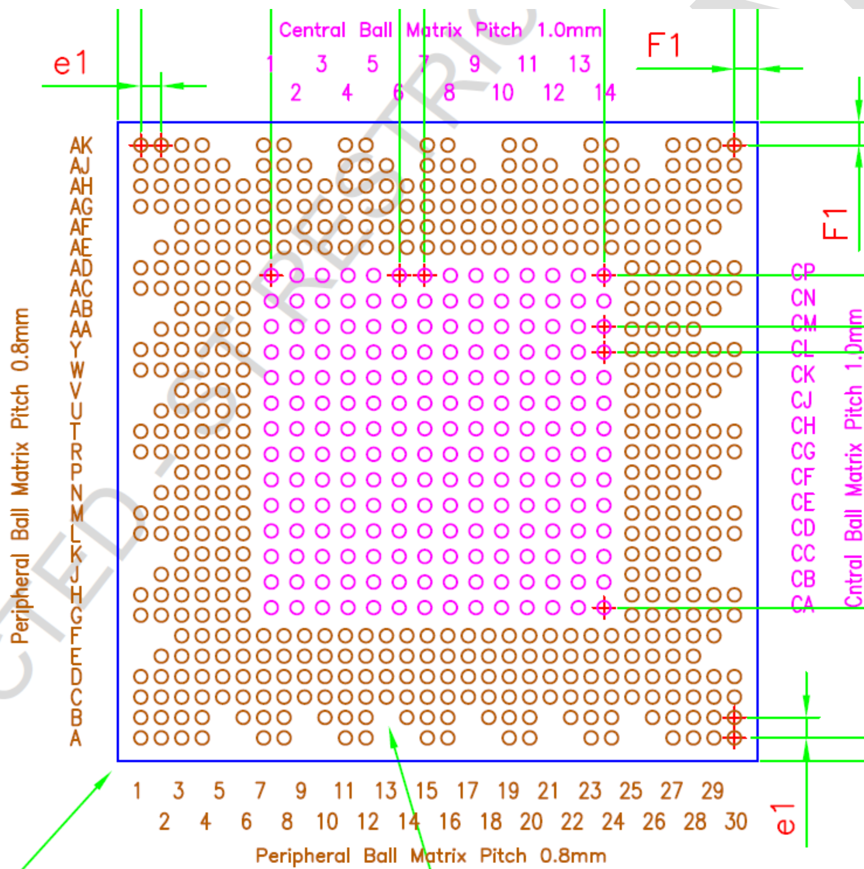
4.2 Test vehicles definition

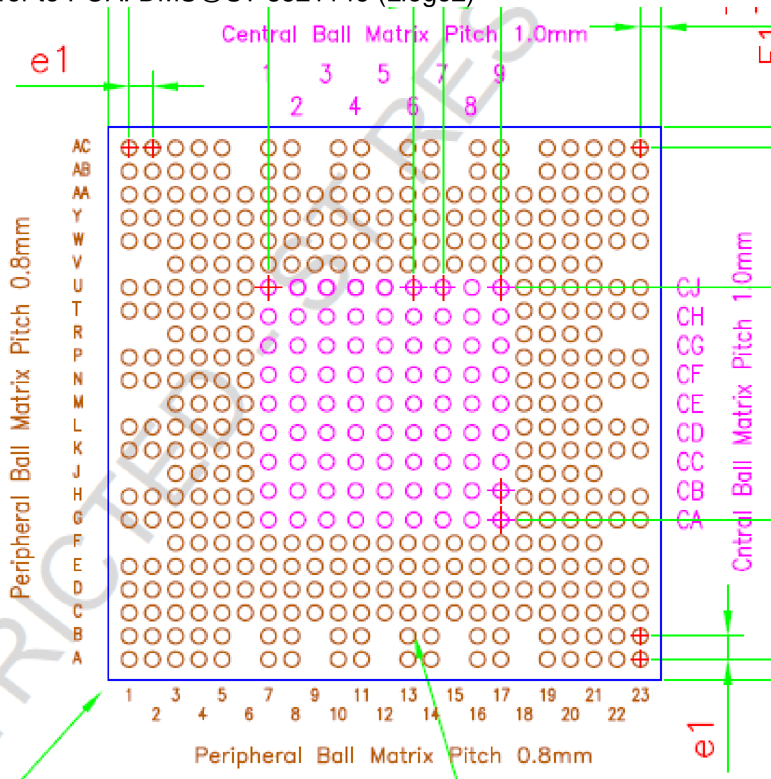
DIE & PRODUCT FEATURES			
Technical code/ Line	H310	*H310*	H32A
Package description	FCBGA 25X25X1.50 700 F30/14 P1/0	*FCBGA19Sqx1.5 449 F23 P.8/1 B0.*	FCBGA16X16X1.32 - 552 P0.65 B0.3
Diffusion process	CMOS028_LP_ISDA	*CMOS028_LP_ISDA*	CMOS028FDSOI_FDY
Wafer fab	Samsung (SEC)		
Wafer diameter	12”		
Wafer thickness (µm)	775 -> 300		
Die front finishing	PEOX + SiN + PIX		PEOX + SiN + PIX
Die back finishing	LAPPED SILICON		LAPPED SILICON
Bumping	Copper pillar		
Bumping house	Winstek (ex- Stats-ChipPAC Taiwan)		
Bump composition & height	Cu/Ni/SnAg 1.8 % 40/3/22µm		

4.3 Package ball out

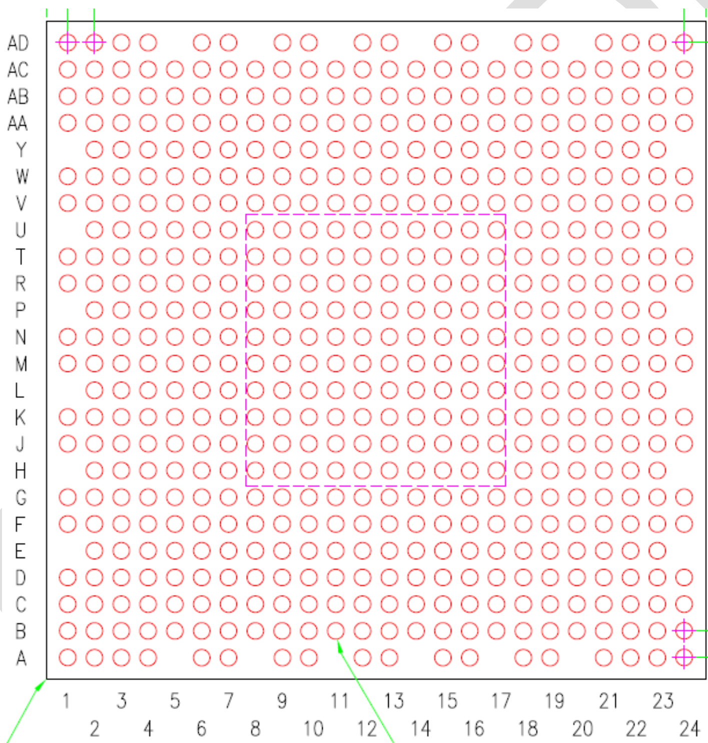
Refer to POA: DMS@ST 8470442 (Cannes2)



Refer to POA: DMS@ST 8521146 (Liege2)



Refer to POA: DMS@ST DM00187128 (L2A)



5 RELIABILITY TEST PLAN

5.1 Sample size required

Trials Sample size per lot:

Temperature cycling 50
High temperature Storage 50
Temperature & Humidity Storage 50

5.2 Lot definition

Lot Nb	Line	Final test location	Reliability location
1	H310 25x25	ST GNB	ST GNB
2	H310 25x25	ST GNB	ST GNB
3	H32A 16x16	ST GNB	ST GNB
4	H32A 16x16	ST GNB	ST GNB

Note: **These lots must be with different top marking for traceability versus the Assembly reports.**
These lots must be manufactured at different days (with different machine set up).
Detailed plan in below chapter will refer to Lot #.

5.3 Test plan summary

Test	Test short description				
	Method	Conditions	SS/Lot	Lot n#	Duration
MSL JL3	Moisture sensitivity level test with JEDEC level 3				
	JEDEC-020	**- SAM (T-SCAN + C-SCAN) @ time 0 on 2x 5 samples per lot - 24h bake @ 125°C - 192h @ 30°C / 60% RH - Reflow simulation (3 times) with standard JEDEC profile @ 260°C peak - SAM (T-SCAN + C-SCAN) after reflow on the same 2x 5 samples per lot**	**150 150 150 150**	1 2 3 4	
MSL+TC	Moisture sensitivity level test followed by Temperature cycling				
	JESD22-A104	**Ta= -40/+125°C Steps: 0, 100, 500, 1000 cycles SAM (T-SCAN + C-SAM) after 1000 cycles on 5 samples per lot**	**50 50 50 50**	1 2 3 4	**1000 cy**
MSL+HTSL	Moisture sensitivity level test followed by High Temperature Storage Life				
	JESD22-A103	**Ta=150°C Steps: 0, 168, 500, 1000 hours SAM (T-SCAN + C-SAM) after 1000 hours No SAM**	**50 50 50 50**	1 2 3 4	**1000 hrs**
MSL+THS	Moisture sensitivity level test followed by Temperature humidity storage				
	JESD22-A118	**Ta=85°C/85%Rh Steps: 0, 168, 500, 1000 hours SAM (T-SCAN + C-SAM) after 1000 hours on 5 samples per lot**	**50 50 50 50**	1 2 3 4	**1000 hrs**

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6 PACKAGE ORIENTED TESTS DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
MSL: Moisture / Reflow Sensitivity Level test	Moisture/Reflow Sensitivity Level test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. Out-of-bag floor life storage and soldering are modeled by the following test sequence: - bake to completely remove moisture from the package; - moisture soak according to the package moisture level; - IR reflow.	It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good representation of the life of the packaged product. The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.
TC: Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, and die attach layer degradation.
HTS: High Temperature Storage	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the maximum operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress voiding.
THS: Temperature Humidity Storage	It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion).	To evaluate the reliability of non-hermetic packaged solid-state devices in humid environments This test is used to identify failure mechanisms internal to the package and is destructive.

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